WHAT IS CLAIMED IS:

1.   For use in a processor having an external memory interface, an instruction prefetch mechanism, comprising:

a branch predictor that predicts whether a branch is to be taken;

prefetch circuitry, coupled to said branch predictor, that prefetches instructions associated with said branch via said external memory interface if said branch is taken and prefetches sequential instructions via said external memory interface if said branch is not taken; and

a loop recognizer, coupled to said prefetch circuitry, that determines whether a loop is present in fetched instructions and reinstates a validity of instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution.

2.   The mechanism as recited in Claim 1 wherein said external memory interface is a synchronous memory interface.

3.   The mechanism as recited in Claim 1 wherein said prefetch circuitry prefetches four of said instructions at a time.

4.   The mechanism as recited in Claim 1 wherein said prefetch

2   circuitry causes said instructions to be placed in a direct mapped

3   instruction cache in said processor.

     5.   The mechanism as recited in Claim 1 wherein said prefetch

2   circuitry drives a request arbiter in said processor.

     6.   The mechanism as recited in Claim 1 wherein said prefetch

2   circuitry is embodied in a state machine.

     7.   The mechanism as recited in Claim 1 wherein said

2   processor is a digital signal processor.

8.   A method of prefetching instructions for a processor,

comprising:

    predicting whether a branch is to be taken;

    prefetching instructions associated with said branch if said

branch is taken;

    prefetching sequential instructions if said branch is not

taken;

    determining whether a loop is present in fetched instructions;

    reinstating a validity of instructions in said loop until said

loop completes execution; and

    preventing said prefetch circuitry from prefetching

instructions outside of said loop until said loop completes

execution.

9.   The method as recited in Claim 8 wherein said prefetching

is carried out via a synchronous memory interface.

10.   The method as recited in Claim 8 wherein said prefetching

is carried out with four of said instructions at a time.

11.   The method as recited in Claim 8 further comprising

causing said instructions to be placed in a direct mapped

instruction cache in said processor.

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12.   The method as recited in Claim 8 further comprising

2   driving a request arbiter in said processor.

13.   The method as recited in Claim 8 wherein said prefetching

2   is carried out in a state machine.

14.   The method as recited in Claim 8 wherein said processor

2   is a digital signal processor.

15. A digital signal processor, comprising:

an execution core having an instruction cache;

a memory unit coupled to said execution core and having an instruction memory and an external memory interface;

a branch predictor, coupled to said instruction cache, that predicts whether a branch is to be taken;

prefetch circuitry, coupled to said branch predictor, that prefetches instructions associated with said branch via said external memory interface if said branch is taken and prefetches sequential instructions via said external memory interface if said branch is not taken; and

a loop recognizer, coupled to said prefetch circuitry, that determines whether a loop is present in fetched instructions and reinstates a validity of instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution.

16. The digital signal processor as recited in Claim 15 wherein said external memory interface is a synchronous memory interface.

17. The digital signal processor as recited in Claim 15 wherein said prefetch circuitry prefetches four of said instructions at a time.

18. The digital signal processor as recited in Claim 15 wherein said prefetch circuitry causes said instructions to be placed in a direct mapped instruction cache in said processor.

19. The digital signal processor as recited in Claim 15 wherein said prefetch circuitry drives a request arbiter in said processor.

20. The digital signal processor as recited in Claim 15 wherein said prefetch circuitry is embodied in a state machine.